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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,805	07/30/2003	Takashi Ozawa	108075-00116	9483

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,805	OZAWA, TAKASHI	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 12-17* is/are rejected.

7)☒ Claim(s) *4-6 and 8-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The present Office action is in response to application dated 30 July 2003.

Claims 1-17 are pending. All claims have been examined.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7 and 12-17are rejected under 35 U.S.C. 103(a) as being unpatentable over Duh et al. [US 2003/0112685 A1] in view of Miyamoto et al. [US 6,810,468 B2].

Regarding claim 1, Duh et al. teaches a FIFO memory (see Figure 1) for use with read and write pointers and read and write clock signals (see Page 4, [0033] and [0034]). The reference also teaches a write counter for updating the write pointer in accordance with the write clock signal and a read counter for updating the read pointer in accordance with the read clock signal (see Page 4, [0034]). Duh et al. also discloses a memory connected to the write and read counter having a plurality of memory cells (see Figure 1, "100", "214", "208", "218"). The memory performs a write operation corresponding to the write pointer and a read operation corresponding to the read pointer (see Page 4, [0032]). Duh et al. also teaches a flag control circuit (see Page 5, [0041], Figure 1, "206") for indicating a memory full condition and a memory empty condition (see Page 4, [0034], "empty condition" and "full condition") synchronously with a clock signal. The reference teaches the flag control circuit (see Figure 1, "206") comparing a write pointer with a read pointer (see Page 5, [0041]).

However, the reference does not teach generating a flag when these pointers match. Regarding this limitation, Miyamoto et al. teaches a FIFO circuit (see Abstract) where an empty flag circuit and a full flag circuit detect whether the pointer values coincide (see col.11, lines 65-67 and col. 12, lines 1-3). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain error detection logic, as taught by Miyamoto et al (see col. 12, lines 15-38).

As for claim 2, Duh et al. does not explicitly teach a first and second comparison circuit for comparing and generating a flag when the read and write pointer match, as claimed. Regarding this limitation, Miyamoto et al. teaches a FIFO circuit (see Abstract) where an empty

flag generating circuit and a full flag generating circuit detect whether the pointer values coincide (see col.11, lines 65-67 and col. 12, lines 1-3). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 3, Duh et al. does not teach a third circuit connected to the write counter and the read counter, for comparing and generating a signal to cancel the flag, as claimed. Regarding this limitation, Miyamoto identifies when the read pointer and the write pointer do not match (see col. 12, lines 34-36). In this case, the error comparing circuit outputs a logical level of "1". At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 7, Duh et al. teaches evaluating an empty condition by comparing the write pointer generated off the write clock signal and a full condition by comparing the read pointer generated off the read clock signal (see Page 5, [0041]). However, the cited reference does not explicitly teach a first and second comparison circuit for comparing and generating a flag when the read and write pointer match, as recited in claim 2. Miyamoto et al. teaches a FIFO circuit (see Abstract) where an empty flag generating circuit and a full flag generating circuit detect whether the pointer values coincide (see col.11, lines 65-67 and col. 12, lines 1-3). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 12, Duh et al. teaches a memory performing write operations in response to the current write pointer and performing read operations in response to the current read pointer (see Page 5, [0041]).

As for claim 13, Duh et al. does not explicitly comparing and generating a flag for the read and write pointers, as claimed. However, the reference does teach a write mode that operates "in-sync" with a write clock signal and a read mode that operated "in-sync" with a read clock signal (See Page 15, claim 1). Regarding these limitations, Miyamoto et al. teaches a FIFO circuit (see Abstract) where an empty flag generating circuit and a full flag generating circuit detect whether the pointer values coincide (see col.11, lines 65-67 and col. 12, lines 1-3). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 14, Duh et al. does teach a write mode that operates "in-sync" with a write clock signal and a read mode that operated "in-sync" with a read clock signal (See Page 15, claim 1). The reference also discusses several examples of a "memory", including shift registers (see Page 1, [0004]). However, the Duh et al. reference does not teach a first or second shift register for sequentially selecting memory cells, as claimed. Regarding this limitation, Miyamoto et al. teaches a FIFO circuit (see Abstract) where an empty flag generating circuit and a full flag generating circuit detect whether pointer values coincide (see col.11, lines 65-67 and col. 12, lines 1-3). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

Regarding claim 15, Duh et al. teaches a FIFO memory (see Figure 1) for use with read and write pointers and read and write clock signals (see Page 4, [0033] and [0034]). The reference also teaches a write counter for updating the write pointer in accordance with the write clock signal and a read counter for updating the read pointer in accordance with the read clock signal (see Page 4, [0034]). Duh et al. also discloses a memory connected to the write and read counter having a plurality of memory cells (see Figure 1, "100", "214", "208", "218"). The memory performs a write operation corresponding to the write pointer and a read operation corresponding to the read pointer (see Page 4, [0032]). Duh et al. also teaches a flag control circuit (see Page 5, [0041], Figure 1, "206") for indicating a memory full condition and a memory empty condition (see Page 4, [0034], "empty condition" and "full condition") synchronously with a clock signal. The reference teaches the flag control circuit (see Figure 1, "206") comparing a write pointer with a read pointer (see Page 5, [0041]).

Duh et al. does not teach a third circuit connected to the write counter and the read counter, for comparing and generating a signal to cancel the flag, as claimed. Regarding this limitation, Miyamoto identifies when the read pointer and the write pointer do not match (see col. 12, lines 34-36). In this case, the error comparing circuit outputs a logical level of "1".

In addition, the Duh et al. reference does not teach generating a flag when these pointers match. Regarding this limitation, Miyamoto et al. teaches a FIFO circuit (see Abstract) where an empty flag circuit and a full flag circuit detect whether the pointer values coincide (see col.11, lines 65-67 and col. 12, lines 1-3).

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

Regarding claim 16, the combination of references teaches or suggests all the limitations corresponding to the FIFO memory for use with read and write pointer and read and write clock signals (see rejections above, *claim 1*). Therefore, the combination of references teaches or suggests all the limitations corresponding to the semiconductor device including the cited memory. Accordingly, the present claim is rejected under the same rationale.

Regarding claim 17, the combination of references teaches or suggests all the limitations corresponding to the FIFO memory for use with read and write pointer and read and write clock signals (see rejections above, *claim 15*). Accordingly, the combination of references teaches or suggests all the limitations corresponding to the semiconductor device including the cited memory. The present claim is rejected under the same rationale.

Claim Objections

5. Claims 4-6, 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, the prior art fails to teach alone or in combination a full flag control circuit, including a *first comparison result determination circuit connected to the third comparison circuit*. In addition, the prior art fails to teach an empty flag control circuit including a *second comparison result determination circuit connected to the third comparison circuit* and

receiving a third signal synchronously with the read clock signal (emphasis added). Claims 5-6 depend upon claim 4 and therefore contain the same allowable limitations.

Regarding claim 8, the prior art fails to teach, alone or in combination a first or second comparison circuit *including a **flip-flop circuit*** having a data output for outputting a signal and a ***reset** input terminal to **feed back a signal delayed by a predetermined time***. The prior art also fails to teach *generating a **pulse signal*** having a ***pulse width** corresponding to the **predetermined delay time*** (emphasis added). Claim 9 depends upon claim 8 and therefore contains the same allowable limitations.

Regarding claims 10 and 11, the prior art fails to teach, alone or in combination a write or read counter containing: (i) *flip-flop circuits* for generating current pointers *synchronously with the clock signal*, the clock signal being controlled by the flag and (ii) *count-up logic circuits connected to the flip-flop circuits* for incrementing the current pointer and generating the next pointer (emphasis added).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Sindalovsky [US 6745265 B1] teaches method and apparatus for generating status flags in a memory device.
- Hikawa [US 5753553 A] teaches a FIFO that requires a full flag and an empty flag, which are generated through comparison of counters (read and write pointers).

- Mc Clure [US 5502655 A] teaches a status flag having a programmable value, which utilizes the same, read and write clocks and reset signals as used by the pointers. The clocks and their complement signals and reset signals are input to read and write counters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on 571-272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
08 August 2005

KIM HUYNH
PRIMARY EXAMINER
8/8/05